In the claims:

1-23. (Cancelled)

24. (New) A method of tuning a voltage controlled oscillator comprising:

dividing a frequency of oscillation of a voltage controlled oscillator to provide a divided frequency of oscillation;

comparing the divided frequency of oscillation to the desired frequency;

providing a tuning voltage based on comparing the divided frequency of oscillation to the desired frequency;

providing a control signal for controlling a change in the frequency of oscillation per change in the tuning voltage; and

applying the control signal to a first terminal of a resistor having a second terminal coupled to a node connecting a first terminal of a first variable capacitor and a first terminal of a second variable capacitor, the first variable capacitor having a second terminal coupled to an inductor; and

applying the tuning voltage to a second terminal of the second variable capacitor.

25. (New) The method of claim 24 wherein each of the first and second variable capacitors is a junction varactor.

26. (New) The method of claim 24 wherein each of the first and second variable capacitors is a MOS varactor.

27. (New) A method of tuning a voltage controlled oscillator comprising:

dividing a frequency of oscillation of a voltage controlled oscillator to provide a divided frequency of oscillation;

comparing the divided frequency of oscillation to the desired frequency;

providing a tuning voltage based on comparing the divided frequency of oscillation to the desired frequency;

providing a control signal for controlling a change in the frequency of oscillation per change in the tuning voltage; and

applying the tuning voltage to a first terminal of a resistor having a second terminal coupled to a node connecting a first terminal of a first variable capacitor and a first terminal of a second variable capacitor, the first variable capacitor having a second terminal coupled to an inductor; and

applying the control signal to a second terminal of the second variable capacitor.

28. (New) The method of claim 24 wherein each of the first and second variable capacitors is a junction varactor.

29. (New) The method of claim 24 wherein each of the first and second variable capacitors is a MOS varactor.

30. (New) A voltage controlled oscillator comprising:

a first inductor;

a first variable capacitor having a first terminal coupled to a first terminal of the first inductor;

a second variable capacitor having a first terminal coupled to a second terminal of the first variable capacitor; and

a first isolation resistor having a first terminal coupled to a node connecting the second terminal of the first variable capacitor and the first terminal of the second variable capacitor and having a second terminal configured to receive a first control voltage,

wherein a second terminal of the second variable capacitor is configured to receive a second control voltage.

31. (New) The circuit of claim 30 wherein the first control voltage is a function of a comparison of a divided frequency of oscillation and a desired frequency.

32. (New) The circuit of claim 31 wherein the second control voltage controls a change in an oscillation frequency of the voltage controlled oscillator per change in the first control voltage.

33. (New) The circuit of claim 32 wherein the first control voltage is a logic signal.

34. (New) The circuit of claim 32 wherein the first control voltage is an analog signal.

35. (New) The circuit of claim 30 wherein the second control voltage is a function of a comparison of a divided frequency of oscillation and a desired frequency.

36. (New) The circuit of claim 35 wherein the first control voltage controls a change in the frequency of oscillation per change in the second control voltage.

37. (New) The circuit of claim 36 wherein the first control voltage is a logic signal.

38. (New) The circuit of claim 36 wherein the first control voltage is an analog signal.

39. (New) The integrated circuit of claim 30 further comprising:

a second inductor;

a third variable capacitor having a first terminal coupled to a first terminal of the second inductor;

a fourth variable capacitor having a first terminal coupled to a second terminal of the third variable capacitor and having a second terminal configured to receive the second control voltage;

a second isolation resistor having a first terminal coupled to a second node connecting the second terminal of the third variable capacitor and the first terminal of the fourth variable capacitor and having a second terminal configured to receive the first control voltage;

a first device having a drain coupled to the first terminal of the first inductor and a gate coupled to the first terminal of the second inductor; and

a second device having a drain coupled to the first terminal of the second inductor and a gate coupled to the first terminal of the first inductor.

40. (New) The circuit of claim 39 further comprising;

a current source coupled to a source of the first device and a source of the second device.

41. (New) The circuit of claim 39 wherein the first device and the second device are n-channel CMOS devices.

42. (New) The circuit of claim 39 wherein each of the first, second, third, and fourth variable capacitors is a junction varactor.

43. (New) The circuit of claim 39 wherein each of the first, second, third, and fourth variable capacitors is a MOS varactor.

44. (New) A phase-locked loop comprising:

a phase detector configured to receive a reference clock and a divided frequency of oscillation;

a low-pass filter coupled to the phase detector and adapted to produce a first control voltage;

a voltage-controlled oscillator coupled to the low-pass filter and adapted to receive the first control voltage and produce a frequency of oscillation; and

a divider adapted to receive the frequency of oscillation and provide the divided frequency of oscillation,

wherein the voltage controlled oscillator comprises:

a first inductor;

a second inductor;

a first variable capacitor having a first terminal coupled to a first terminal of the first inductor;

a second variable capacitor having a first terminal coupled to a first terminal of the second inductor;

a third variable capacitor having a first terminal coupled to a second terminal of the first variable capacitor and having a second terminal configured to receive a second control voltage;

a fourth variable capacitor having a first terminal coupled to a second terminal of the second variable capacitor and having a second terminal configured to receive the second control voltage;

a first isolation resistor having a first terminal coupled to a first node connecting the second terminal of the first variable capacitor and the first terminal of the third variable capacitor and having a second terminal configured to receive the first control voltage;

a second isolation resistor having a first terminal coupled to a second node connecting the second terminal of the second variable capacitor and the first terminal of the fourth variable capacitor and having a second terminal configured to receive the first control voltage;

a first device having a drain coupled to the first terminal of the first inductor and a gate coupled to the first terminal of the second inductor; and

a second device having a drain coupled to the first terminal of the second inductor and a gate coupled to the first terminal of the first inductor.

45. (New) The phase lock loop of claim 44 wherein the voltage controlled oscillator further comprises one or more capacitive circuits each comprising:

a fifth variable capacitor having a first terminal coupled to the first terminal of the first inductor;

a sixth variable capacitor having a first terminal coupled to the first terminal of the second inductor;

a seventh variable capacitor having a first terminal coupled to a second terminal of the fifth variable capacitor and having a second terminal configured to receive the second control voltage;

an eighth variable capacitor having a first terminal coupled to a second terminal of the sixth variable capacitor and having a second terminal configured to receive the second control voltage;

a third isolation resistor having a first terminal coupled to a third node connecting the second terminal of the fifth variable capacitor and the first terminal of the seventh variable

capacitor and having a second terminal configured to receive one of one or more additional control voltages;

a second isolation resistor having a first terminal coupled to a fourth node connecting the second terminal of the sixth variable capacitor and the first terminal of the eighth variable capacitor and having a second terminal configured to receive the one of the one or more additional control voltages.

46. (New) The phase lock loop of claim 45 further comprising control logic adapted to provide the one or more additional control voltages.

47. (New) The phase lock loop of claim 44 wherein the first device and the second device are n-channel CMOS devices.

48. (New) The phase lock loop of claim 44 wherein the first, second, third, and fourth variable capacitors are junction varactors.

49. (New) The integrated circuit of claim 44 wherein the first, second, third, and fourth capacitors are MOS varactors.